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EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

CH

Office Action Summary	Application No.	Applicant(s)	
	10/024,119	YUFFE ET AL.	
	Examiner	Art Unit	
	James H. Cho	2819	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12-17-2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-13,15,21-25 and 28* is/are rejected.

7)☒ Claim(s) *7,8,15,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1, 6, 11, 16 and 21 are objected to because of the following informalities:

In claim 1, the wording, "unit to" on lines 5 and 9 appears to be --unit is to-- respectively;

In claims 1, 11, 16 and 21, the wording, "(AGTL)-type bus" on line 3, line 3, line 4, and lines 2-3 appears to be --(AGTL) bus-- respectively, because the wording, "type" in claim is unclear and indefinite; and

In claim 6, the wording, "of claim 4" appears to be --of claim 5--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 9-10, 11, 13, 15, 21, 23-25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara (US PAT No. 5,731,711).

Regarding claims 1 and 11, Fig. 5 of Gabara teaches a circuit (300) comprising: a first switch unit or means (340) connectable to a first power line (V_{DDQ}), a control line (line to the gate of 340), a bus line (bus connected to 301, i.e. 115 as shown in Fig. 3) of an assisted Gunning transceiver logic bus (col. 9, lines 37-67), the first switch unit

having an impedance (Z_0) that substantially matches the characteristic impedance of the bus line (col. 10, lines 57-59), where the first switch unit is to electrically connect the first power line and the bus line when enabled by a control signal (I/O) received by the control line; and a second switch unit or means (360) connectable to a second power line (Vss) and the bus line, the second switch unit having an impedance (desired impedance $Z_{0/3}$; col. 10, lines 54-57) different from that of the first switch unit, where the second switch unit is to electrically connect a second power line (Vss) and the bus line when enabled, the second switch unit to be disabled when the first switch unit is enabled and to be enabled when the first switch unit is disabled (activations of 340 and 360 are complementary each other; col. 10, line 60 - col. 11, line 30).

Regarding claim 3, Fig. 5 of Gabara teaches the circuit of claim 1, further comprising an amplifier (INPUT BUFFER, i.e. 105 as shown in Fig. 3; buffer is an amplifier with a unit gain).

Regarding claims 4 and 13, Fig. 5 of Gabara teaches the circuit of claims 1 and 11, where the first switch unit comprises a P-channel transistor (340 is PMOS).

Regarding claims 5 and 15, Fig. 5 of Gabara teaches the circuit of claims 4 and 13, where the first switch further comprises a resistor (Z_0 in Fig. 6B) connected in series with the P-channel transistor (col. 11, lines 43-46).

Regarding claims 9 and 13, Fig. 5 of Gabara teaches the circuit of claims 1 and 11, where the second switch unit comprises an N-channel transistor (360 is NMOS).

Regarding claim 10, Fig. 5 of Gabara teaches the circuit of claim 9, where the second switch unit further comprises a resistor ($Z_{0/3}$ in Fig. 6B) connected in series with the N-channel transistor (col. 11, lines 55-59).

Regarding claim 21, Fig. 5 of Gabara teaches a system comprising: an assisted Gunning transceiver logic bus (bus coupled to 301, i.e. 115 as shown in Fig. 3), a first driver/receiver circuit (100 in Fig. 3) coupled to one end of a bus line of the AGTL bus, the first driver/receiver circuit including a first pull-up switch unit (340 in Fig. 5) to coupled a first power line (V_{DDQ}) to the bus line to the bus line where the first pull-up switch unit has an impedance substantially matching the bus line's characteristic impedance (co. 10, lines 57-59), a first pull-down switch unit (360 in Fig. 5) coupled to a first ground line (Vss in Fig. 5), where the first pull-down switch unit has an impedance different from that of the first pull-up switch unit (desired impedance $Z_{0/3}$; col. 10, lines 54-57) and a second driver/receiver circuit (150 in Fig. 3) coupled to another end of the bus line, the second driver/receiver circuit including a second pull-up switch unit (340 in Fig. 5 implemented in 150 in Fig. 3) to coupled a second power line (V_{DDQ}) to the bus line to the bus line, the first and second power lines having substantially identical voltage levels (V_{DDQ} in 100 and V_{DDQ} in 150 are the same) where the second pull-up switch unit has an impedance substantially matching to that of the first pull-up switch

unit (co. 10, lines 57-59), a second pull-down switch unit (360 in Fig. 5) coupled to a second ground line (Vss in Fig. 5 implemented in 150 of Fig. 3), the first and second ground lines having substantially identical voltage levels (Vss in Fig. 5 implemented in 100 in Fig. 3 is the same as Vss implemented in 150 in Fig. 3) where the second pull-down switch unit has an impedance substantially matching that of the first pull-down switch unit (desired impedance $Z_{0/3}$; col. 10, lines 54-57).

Regarding claim 23, Figs. 3 and 5 of Gabara teaches the system of claim 21 where the first and second driver/receiver circuits each further comprise an amplifier (INPUT BUFFER, i.e. 105 as shown in Fig. 3; buffer is an amplifier with a unit gain) having an input terminal connected to the bus line (input terminal of 105s in 100 and 150 in Fig. 3).

Regarding claim 24, Figs. 3 and 5 of Gabara teaches the system of claim 21 where the first pull-up switch unit comprises a P-channel having one terminal coupled to the first power line (340 in Fig. 5 is PMOS).

Regarding claim 25, Figs. 3 and 5 of Gabara teaches the system of claim 21, where the first pull-up switch unit further comprises a resistor (Z_0 in Fig. 6B) connected in series with the P-channel transistor (col. 11, lines 43-46).

Regarding claim 28, Figs. 3 and 5 of Gabara teaches the system of claim 21, where the first pull-down switch unit comprises an N-channel transistor (360 is NMOS).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara (US PAT No. 5,731,711).

Regarding claims 2, 12 and 22, Figs. 3, 5 and 6B of Gabara discloses the circuit of claims 1, 11 and 22 where the second unit's impedance is one-third of the first switch unit but does not disclose the second unit's impedance is half of the first switch unit. However, Gabara discloses the terminating impedance for the second unit is a user defined (col. 10, lines 51-59) for the purpose of providing a desired impedance.
It would have been obvious at the time the invention was made to a person having ordinary skill in the art to construct the impedance of the second unit's impedance of Gabara to be a half of the first switch unit because it would provide the designer's choice of the impedance.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gabara (US PAT No. 5,731,711) in view of Jones et al. (US PAT No. 6,351,136).

Regarding claim 6, Fig. Figs 3 and 5 of Gabara teaches the circuit of claim 4 where the resistor and a switch is coupled in series, but does not disclose the resistor being a N-well resistor. However, Figs, 2A and 2B of Jones et al. teaches a discrete resistor implemented with a transistor having N-well since it is inherent that a transistor is utilized as a resistor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to construct the discrete resistor of Gabara with n-well resistor of Jones et al. because it is well known in the art as taught in the Jones et al.

5. Method claims 16-20 are essentially the same in scope as apparatus claims 1-6, 9-13, 15, 21-25, and 28 and are rejected similarly.

Allowable Subject Matter

6. Claims 7-8, 14 and 26-27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as well as including all corrections of claim objection stated above.

The following is an examiner's statement of reasons for the indication of allowable subject matter: Although, Gabara teaches a controllable impedance arrangement used in an adaptable input-output port of an integrated circuit providing different specific impedances for transmitting signals at respective signal levels, or a terminating impedance when receiving a data signal, and Jones et al. teaches an n-well resistor, one of ordinary skill in the art would not have been motivated to modify the teachings of Gabara and/or Jones et al. to further include, among other things, the

specifics of a trim circuit coupled to PMOS switch unit where the trim circuit adjusts the impedance of the PMOS switch unit to a reference impedance after comparing the with the reference impedance, etc., as set forth in the claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Williams (US PAT No. 6,222,389) discloses assisted Gunning transceiver logic bus driver.

Stoenner (US PAT No. 6,054,881) discloses I/O buffer selectively providing resistive termination for a transmission line.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

James H. Cho
Examiner
Art Unit 2819

August 11, 2003